

FEATURES

- Meets or Exceeds the Requirements of IBM[®] 360/370 Input/Output Interface Specification for 4.5-Mb/s Operation
- Single 5-V Supply •
- **Uncommitted Emitter-Follower Output** Structure for Party-Line Operation
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible With** TTL
- Receiver Input Resistance . . . 7.4 k Ω to 20 k Ω
- **Ratio Specification for Propagation Delay** Time, Low to High/High to Low

DESCRIPTION/ ORDERING INFORMATION

The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It also is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 drive terminated lines, such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

An open line affects the receiver input as does a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line by pulling either DE1 or DE2 to a low level.

D OR N PACKAGE (TOP VIEW)							
DE1	[]	υ	4.0				
DEI	11		16	Vcc			
RI1 [2		15	DO1			
RO1 [3		14] DI1			
RI2 [4		13	002			
RO2 [5		12] DI2			
RI3 [6		11	DO3			
RO3 [7		10] DI3			
GND [8		9	DE2			

DW PACKAGE (TOP VIEW)

DE1	1	\cup_{20}	h	Vcc	
RI1 [2	19	Б	DO1	
N.C. [3	18	þ	N.C.	
R01 [4	17	þ	DI1	
RI2 [5	16		DO2	
RO2 [6	15	6	DI2	
RI3 [7	14	b	DO3	
N.C. [8	13	b	N.C.	
RO3 [9	12	þ	DI3	
GND [10	11	þ	DE2	

NS PACKAGE (TOP VIEW)

		∇	_
DE1	U 1	20	V _{cc}
RI1] 2	19	DO1
RO1] 3	18	DI1
RI2	4	17] DO2
N.C.	Q 5	16] N.C.
N.C.	6	15] N.C.
RO2	[7	14] DI2
RI3	8]	13] DO3
RO3	9	12] DI3
GND	10	11] DE2

N.C. - No internal connection



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ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube	SN751730N	SN751730N	
	SOIC – D	Tube	SN751730D	SN751730	
0°C to 70°C	3010 - 0	Tape and reel	SN751730DR	31/31/30	
		Tube	SN751730DW	SN751730	
	SOIC – DW	Tape and reel	SN751730DWR	SN751730	
	SOP – NS	Tape and reel	SN751730NSR	SN751730	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

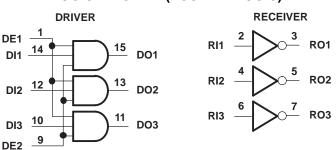
EACH DRIVER

	INPUTS	OUTPUT	
DI	DE1	DE2	DO
L	Х	Х	L
х	L	Х	L
х	х	L	L
Н	н	н	н

EACH DRIVER⁽¹⁾

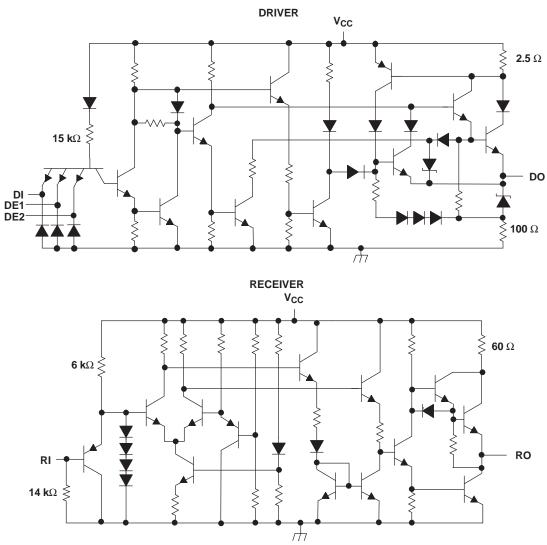
INPUT RI	OUTPUT RO
L	Н
н	L
Open	Н

(1) H = high level, L = low level, X = irrelevant



LOGIC DIAGRAM (POSITIVE LOGIC)

Pin numbers shown are for the D and N package only.



EQUIVALENT SCHEMATICS OF DRIVER AND RECEIVER⁽¹⁾

(1) All resistor values are nominal.

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			7	V
V	Input voltogo rongo	Driver	-0.5	7	V
V _{CC} V _I V _O θ _{JA} T _J	Input voltage range	Receiver	-0.5	7	V
Vo	Output voltage range	Driver	-0.5	7	V
	Enable input voltage range			7	V
	- (3)	D package		73	
~		DW package		58	0000
θ _{JA}	Package thermal impedance ⁽³⁾	N package		67	°C/W
		NS package		60	
TJ	Operating virtual junction temperature			150	°C
	Lead temperature 1,6 mm (1/16 inch) fr	om case for 10 s		260	°C
T _{stg}	Storage temperature range		-65	150	°C/W

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. (1)

All voltage values are with respect to network ground terminal. (2) (3)

The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _{IH} High-level input voltage	Driver, Enable	2			V	
	High-level input voltage	Receiver	1.55			v
V		Driver, Enable			0.8	
VIL	Low-level input voltage	Receiver			1.15	V
T _A	Operating free-air temperature		0		70	°C



DRIVER SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST C	TEST CONDITIONS			UNIT		
V _{IK}	Input clamp voltage		V _{CC} = 4.75 V,	$I_{IL} = -18 \text{ mA}$		-1.5	V		
			V _{CC} = 4.75 V, I _{OH} = -59.3 mA	$V_{IH} = 2 V,$ $T_A = 25^{\circ}C$	3.11				
V _{OH}	High-level output voltage		$V_{CC} = 5.25 \text{ V},$ $I_{OH} = -78.1 \text{ mA}$	V _{IH} = 2 V,		4.1			
	nigimevel output voitage		$\begin{array}{l} V_{CC} = 4.75 \; V, \\ R_{L} = 51.4 \; \Omega \end{array}$	V _{IH} = 2 V,	3.05		V		
			$\begin{array}{l} V_{CC} = 5.25 \; V, \\ R_{L} = 56.9 \; \Omega \end{array}$	V _{IH} = 2 V,		4.2			
V _{ODH}	Differential high-level output voltage		R_L = 46.3 Ω or 56.9 Ω			0.5	V		
			V _{CC} = 5.25 V,	I _{OL} = -0.24 mA		0.15			
V _{OL}	Low-level output voltage		rel output voltage $V_{IL} = 0.8 V,$ $V_{IH} = 4.5 V$	$R_L = 56.9 \ \Omega$		0.15	V		
	High-level input current	DI		V _{IH} = 2.7 V		20			
IIH	High-level linput current	DE	V _{CC} = 5.25 V,			60	μA		
	Low-level input current	DI	V _{CC} = 5.25 V,	V _{IH} = 0.4 V		-400	μA		
IIL	Low-level input current	DE	$v_{\rm CC} = 5.25 \ v_{\rm cc}$	$v_{\rm IH} = 0.4 v$		-1200	μΑ		
	High-level output current		V _{CC} = 4.75 V,	$V_{IL} = 0$		100	μA		
I _{OH}	High-level bulput current		$V_{OH} = 5 V$	V _{IH} = 4.5 V		100	μΑ		
I _{OS}	Short-circuit output current ⁽¹⁾		$V_{CC} = 5.25 V$	V _{IH} = 4.5 V		-30	mA		
I _{CCH}	Supply current (total package)			$V_{cc} = 5.25 V_{cc}$	V _{CC} = 5.25 V,			47	
I _{CCL}			No load	$V_{I(D)} = 0,$ $V_{I(R)} = 4.5 V$		80	mA		

(1) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics

 $V_{CC} = 5 V + 5\%, T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output			6.5	12	18.5	ns
t _{PHL}	Propagation delay time, high- to low-level output	$R_L = 47.5 \ \Omega,$	See Figure 1	6.5	12	18.5	ns
Δt_{pd}	Differential propagation delay time ⁽¹⁾		-			10	ns
t _r	Output rise time	$V_{CC} = 5 V,$	V _O = 0.15 V to 3.05	5	10		ns
t _f	Output fall time	$R_L = 47.5 \Omega$, See Figure 1	V, C _L = 10.2 pF,	5	13		ns
SR	Slew rate	$\label{eq:V_O} \begin{array}{l} V_O = 1 \ V \ \text{to} \ 3 \ V \\ \text{average}, \\ R_L = 47.5 \ \Omega, \\ \text{See Figure 1} \end{array}$	C _L = 10.2 pF,			0.65	V/ns

(1) $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

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RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TI	TEST CONDITIONS		MAX	UNIT
V _{OH}	High-level output voltage	V _{CC} = 4.75 V, _{IOH} = -400 μA	V _I = 1.15 V,	2.7		V
		V _{CC} = 4.75 V,	I _{OL} = 8 mA		0.5	V
V _{OL}	Low-level output voltage	V _{IH} = 1.55 V	$I_{OL} = 4 \text{ mA}$		0.4	V
r _l	Input resistance	$V_{CC} = 0,$	V ₁ = 0.15 V to 3.9 V	7.4	20	kΩ
I _{IH}	High-level input current	V _{CC} = 4.75 V,	V _{IH} = 3.11 V		0.42	mA
IIL	Low-level input current	V _{CC} = 5.25 V,	V _{IL} = 0.15 V	-0.24	0.04	mA
$I_{OS}^{(1)}$	Short-circuit output current	V _{CC} = 5.25 V,	$V_{IL} = 0$	-20	-100	mA
I _{CCH}	Supply current (total	V _{CC} = 5.25 V,	$V_{I(D)} = 4.5 V,$ $V_{I(R)} = 0$		47	٣A
I _{CCL}	package)	No load	$V_{I(D)} = 0,$ $V_{I(R)} = 4.5 V$		80	mA

(1) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics

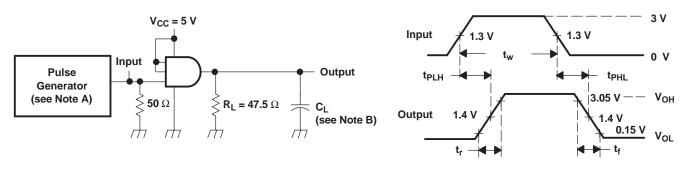
 $V_{CC} = 5 V + 5\%, T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	$R_L = 2 k\Omega$, $C_L = 15 pF$, See Figure 2	7.5	12	19.5	ns
t _{PHL}	Propagation delay time, high- to low-level output		7.5	12	19.5	ns
$\Delta t_{pd}^{(1)}$	Differential propagation delay time				10	ns

(1) $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

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PARAMETER MEASUREMENT INFORMATION

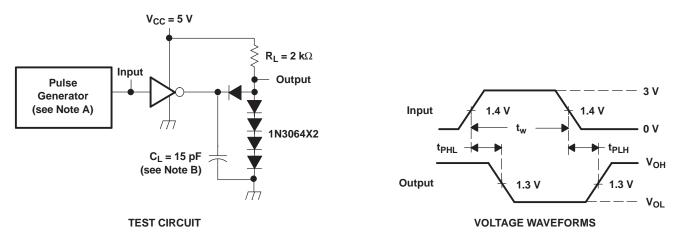


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50 \ \Omega$, $t_w \le 500 \ ns$, PRR $\le 1 \ MHz$, $t_f \le 6 \ ns$, $t_r \le 15 \ ns$. B. C_L includes probe and jig capacitance.





NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50 \ \Omega$, $t_w \le 500 \text{ ns}$, PRR $\le 1 \text{ MHz}$, $t_f \le 10 \text{ ns}$, $t_r \le 10 \text{ ns}$. B. C_L includes probe and jig capacitance.

Figure 2. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN751730D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN751730NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN751730NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN751730NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

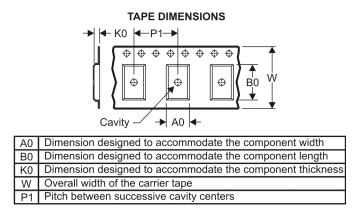
13-Jul-2007

to Customer on an annual basis.

TEXAS INSTRUMENTS www.ti.com

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

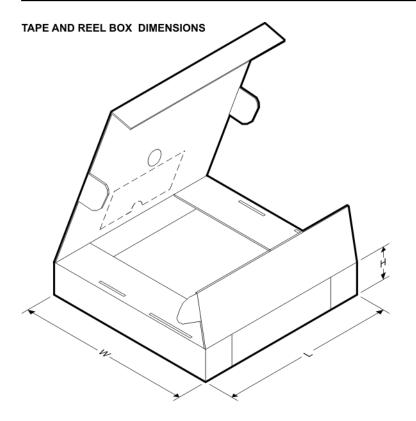


*Al	l dimensions are nominal												
	Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN751730DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
	SN751730NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN751730DR	SOIC	D	16	2500	333.2	345.9	28.6
SN751730NSR	SO	NS	20	2000	346.0	346.0	41.0

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

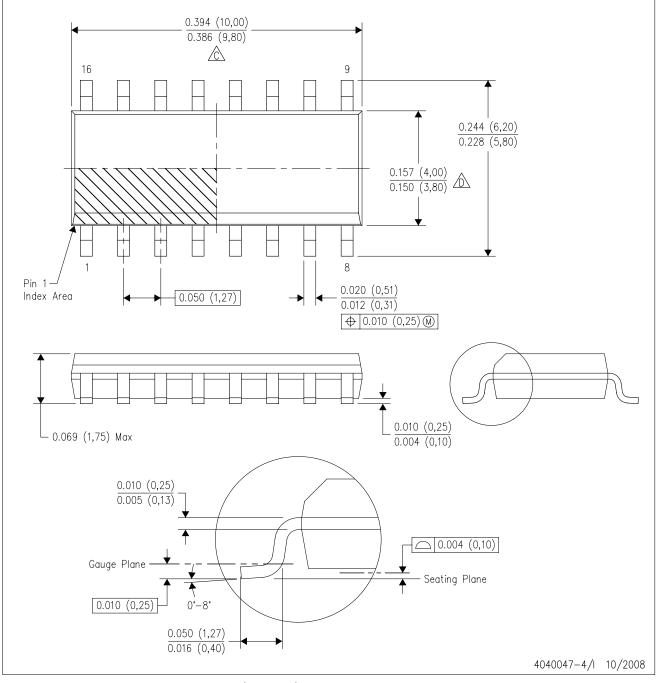
14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

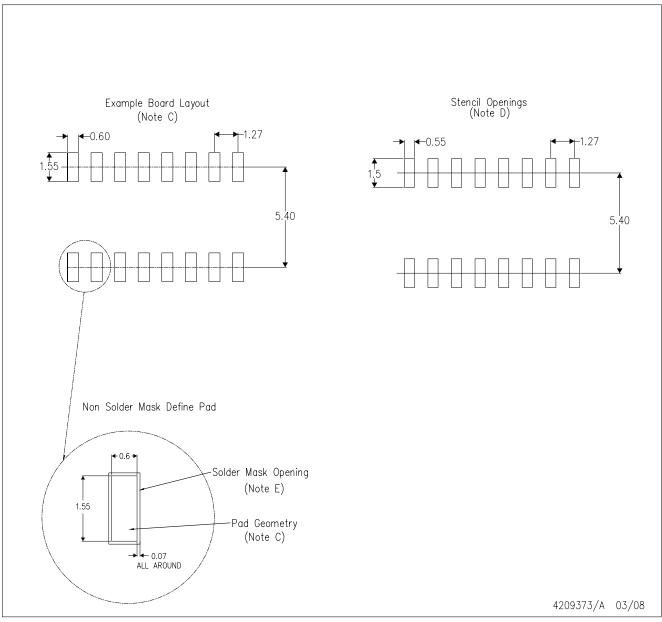


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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